IN THE CLAIMS

Please cancel claims 1-10 and add new claims 11 and 12 as follows.

1-10 (Cancelled).

11. (New) A multiple processor integrated circuit comprising:

a first processor coupled to a first cache;

a first interface coupled to receive memory references that miss in the first cache;

a second processor coupled to a second cache;

a second interface coupled to receive memory references that miss in the second cache;

common circuitry coupled to the first interface and to the second interface;

a first power terminal coupled to provide power to the first processor;

a second power terminal coupled to provide power to the second processor;

a third power terminal coupled to provide power to the common circuitry;

wherein the common circuitry comprises a memory bus interface;

wherein the first interface is configured to permit operation of the second processor when the first power terminal is not powered;

wherein the second interface is configured to permit operation of the first processor when the second power terminal is not powered; and

wherein the first interface is designed such that no signals driven by gates powered by the third power terminal are connected to any P-diffusion located in an N-well that is electrically connected to the first power terminal.

12. (New) The processor integrated circuit of claim 11, wherein the first interface is designed such that no signals driven by gates powered by the third power terminal are connected to any P-diffusion located in an N-well that is electrically connected to the second power terminal.